REMARKS

The specification has been amended. Claims 1-15 are pending, with claims 1, 10, and 14-15 being independent.

Attached hereto is an Appendix entitled "Version with Markings to Show Changes Made" which is a marked-up version of the portions of the application which have been amended by the present amendment, with underlining indicating added matter.

A preliminary amendment was filed on October 15, 2001, but the Office Action of January 25, 2002, does not indicate that the preliminary amendment of October 15, 2001, has been entered. Accordingly, it is respectfully requested that the Examiner specifically indicate on the record in the next Office communication that the preliminary amendment of October 15, 2001, has been entered.

The present application is a continuation of application Serial No. 09/043,534 filed on March 20, 1998, which is a national stage application under 35 USC 371 of international application No. PCT/JP95/01886 filed on September 20, 1995, as indicated in the new section entitled "CROSS-REFERENCES TO RELATED APPLICATIONS" which was added on page 1 of the specification in the preliminary amendment of October 15, 2001, as required by 35 USC 120. However, the Examiner did not check the box in item 15 on page 1 (the Office Action Summary) of the Office Action of January 25, 2002, to acknowledge the claim for domestic priority under 35 USC 120. Accordingly, it is respectfully requested that the Examiner

acknowledge the claim for domestic priority under 35 USC 120 in the next Office communication.

At the bottom of page 2 of the Office Action of January 25, 2002, the Examiner states that **"Any response to this final action should be mailed to . . . ."**. However, it is submitted that the Office Action of January 25, 2002, is in fact a non-final Office Action as indicated in item 2b on page 1 (the Office Action Summary) of the Office Action of January 25, 2002.

Claims 1-15 were rejected under 35 USC 101 as claiming the same invention as that of claims 1-16 of U.S. Patent No. 6,329,973 which issued from parent application Serial No. 09/043,534 of the present application. This rejection is respectfully traversed.

In explaining the rejection, the Examiner states as follows:

> The term "AND functional circuit" in the independent claims of the present application and the term "AND logical circuit" in the allowed independent claims of the prior U.S. Patent No. 6,329,973 are directed to the same AND gate circuit, therefore, claims 1-15 of the present application are claiming the same invention as that of claims 1-16 of prior U.S. Patent No. 6,329,973.

Claims 1-15 of the present application are respectively identical to claims 1-9 and 11-16 of U.S. Patent No. 6,329,973, except that the term AND logical circuit in the last paragraph of independent patent claims 1, 11, and 15-16 has been changed to AND functional circuit in independent application claims 1, 10, and 14-15 which respectively

correspond to independent patent claims 1, 10, and 15-16. It is noted that independent patent claim 10 does not recite an AND logical circuit as do independent patent claims 1, 11, and 15-16, and accordingly it is submitted that independent patent claim 10 should not have been included in the statement of the rejection.

The Examiner's position that application claims 1-15 claim the same invention as that of patent claims 1-9 and 11-16 appears to be based on the Examiner's position that the AND functional circuit recited in independent application claims 1, 10, and 14-15 and the AND logical circuit recited in independent patent claims 1, 11, and 15-16 read on AND gate circuit 47 shown, for example, in Fig. 1 and described, for example, on page 8, lines 21-22, of the specification as originally filed.

However, it is submitted that the proper test of whether application claims 1-15 claim the same invention as that of patent claims 1-9 and 11-16 is set forth in MPEP 804, Eighth Edition, August 2001, pp. 800-20 to 800-21, which provides as follows in pertinent part (emphasis added):

> ***A. Statutory Double Patenting — 35 U.S.C. 101***
>
> In determining whether a statutory basis for a double patenting rejection exists, the question to be asked is: Is the same invention being claimed twice? 35 U.S.C. 101 prevents two patents from issuing on the same invention. "Same invention" means identical subject matter. *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1984); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957).

> A reliable test for double patenting under 35 U.S.C. 101 is whether a claim in the application could be literally infringed without literally infringing a corresponding claim in the patent. *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970). Is there an embodiment of the invention that falls within the scope of one claim, but not the other? If there is such an embodiment, then identical subject matter is not defined by both claims and statutory double patenting would not exist. For example, the invention defined by a claim reciting a compound having a "halogen" substituent is not identical to or substantively the same as a claim reciting the same compound except having a "chlorine" substituent in place of the halogen because "halogen" is broader than "chlorine." On the other hand, claims may be differently worded and still define the same invention. Thus, a claim reciting a widget having a length of "36 inches" defines the same invention as a claim reciting the same widget having a length of "3 feet."

Here, it is submitted that the term AND functional circuit recited in independent application claims 1, 10, and 14-15 is broader than the term AND logical circuit recited in independent patent claims 1, 11, and 15-16, such that there are embodiments of the invention which fall within the scope of application claims 1-15 but do not fall within the scope of patent claims 1-9 and 11-16.

For example, it is submitted that the term AND functional circuit recited in independent application claims 1, 10, and 14-15 means any circuit which performs an AND function, while the term AND logical circuit recited in independent patent claims 1, 11, and 15-16 means a logical circuit which performs an AND function.

Attached hereto is a copy of H. Taub et al., Digital Integrated Electronics, 1977, p. 440 (the first page of Chapter 13, "Analog Switches", as indicated on page xiv of the table of contents), McGraw-Hill, New York, ISBN 0-07-062921-8, which states as follows in pertinent part (emphasis added):

> Digital waveforms, ideally at least, make abrupt transitions between two separated ranges of values. One range represents logic level **1** while the other range represents logic level **0**. Within each range, the exact signal level is of no significance. In logical gates all inputs and outputs are digital signals.

In light of this, it is submitted that one of ordinary skill in the art might arguably interpret the term AND logical circuit recited in independent patent claims 1, 11, and 15-16 to mean a logical circuit which performs an AND function and is implemented with a digital circuit.

In contrast, it is submitted that one of ordinary skill in the art would understand that the term AND functional circuit recited in independent application claims 1, 10, and 14-15 is not limited to an implementation with a digital circuit, but means any circuit which performs an AND function, and may be implemented with either a digital circuit, or with an analog circuit, such as, for example, an operational amplifier.

Accordingly, it is submitted that an embodiment of the present invention including an analog circuit which performs an AND function would fall within the scope of independent application claims 1, 10, and 14-15 and dependent application claims 2-9 and 11-13 depending from independent application

claims 1 and 10, but would arguably not fall within the scope of independent patent claims 1, 11, and 15-16 and dependent application claims 2-9 and 12-14 depending from independent patent claims 1 and 11 because, as discussed above, one of ordinary skill in the art might arguably interpret the term AND logical circuit recited in independent patent claims 1, 11, and 15-16 to mean a logical circuit which performs an AND function and is implemented with a digital circuit.

Accordingly, it is submitted that claims 1-15 of the present application do not claim the same invention as that of claims 1-16 of U.S. Patent No. 6,329,973 under the test set forth in MPEP 804, such that claims 1-15 of the present application are not subject to a double patenting rejection under 35 USC 101 over claims 1-16 of U.S. Patent No. 6,329,973.

Since claims 1-15 of the present application do not claim the same invention as that of claims 1-16 of U.S. Patent No. 6,329,973 for the reasons discussed above, it is respectfully requested that the rejection of claims 1-15 under 35 USC 101 as claiming the same invention as that of claims 1-16 of U.S. patent No. 6,329,973 be withdrawn.

As recognized by the Examiner, the other references cited but not relied upon neither disclose nor suggest the present invention, and thus no further discussion of these other references is deemed necessary at this time.

It is submitted that the Examiner's only rejection has been overcome, and that the application is now in condition

for allowance. Reconsideration of the application and an action of a favorable nature are respectfully requested.

To the extent necessary, the applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, or credit any overpayment of fees, to the deposit account of Antonelli, Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (520.36114CX1).

Respectfully submitted,

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Attachments

APPENDIX

VERSION WITH MARKINGS TO SHOW CHANGES MADE

Changes made to the application by the present amendment are indicated below, with underlining indicating added matter.

IN THE SPECIFICATION

The new section entitled "CROSS-REFERENCES TO RELATED APPLICATIONS" which was added on page 1 between line 2 ("IMAGE DISPLAY") and line 3 ("BACKGROUND OF THE INVENTION") in the preliminary amendment of October 15, 2001, and has been deleted and replaced with the following replacement section:

--CROSS-REFERENCES TO RELATED APPLICATIONS

This application is a continuation of application Serial No. 09/043,534 filed on March 20, 1998, now U.S. Patent No. 6,329,973, which is a national stage application under 35 USC 371 of international application No. PCT/JP95/01886 filed on September 20, 1995.--

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11.8 Complementary Numbers 371
11.9 Representation of Signed Numbers in Registers 374
11.10 Subtraction Through Complementation and Addition 376
11.11 Twos-complement Addition and Subtraction 377
11.12 Ones-complement Addition and Subtraction 378
11.13 Addition and Subtraction of a Sequence of Signed Numbers 380
11.14 A Saturating Adder 381
11.15 Scaling 383
11.16 Multiplication 386
11.17 Division 387
11.18 The Arithmetic Logic Unit (ALU) 389

12 Semiconductor Memories **392**

12.1 Type of Memories 392
12.2 Shift-Register Sequential Memories 394
12.3 MOS Register Stages 396
12.4 Two-Phase Ratioless Shift Register 400
12.5 Four-Phase Ratioless Register Stage 402
12.6 CMOS Register Stages 403
12.7 Static Shift-Register Stage 405
12.8 A Three-Phase Static Register Stage 407
12.9 The Read-Only Memory 409
12.10 Implementation of ROMs 412
12.11 Programmable and Eraseable ROMs 413
12.12 Applications of ROMs 413
12.13 Bipolar-Junction-Transistor Random-Access-Memory Cells 416
12.14 Other Bipolar-Transistor Memory Cells 418
12.15 MOS RAMs 420
12.16 Organization of a RAM 425
12.17 Paralleling of Semiconductor Memory Integrated-Circuit Chips 427
12.18 The Charged-Coupled Device (CCD) 431
12.19 Storage of Charge 433
12.20 Transfer of Charge 434
12.21 Input and Output Arrangement 437

13 Analog Switches **440**

13.1 Basic Operating Principles of Analog Gates 441
13.2 Applications of Switching Circuits 442
13.3 Diode Transmission Gates 451
13.4 Bipolar Junction Transistor Gates 463
13.5 FET Gates 466
13.6 Operational Amplifiers 467
13.7 An FET Gate with an Op-Amp Load 468
13.8 A Sample-and-Hold Circuit 470
13.9 FET Gate Drivers 476
13.10 CMOS Gates 479

13

ANALOG SWITCHES

Digital waveforms, ideally at least, make abrupt transitions between two separated ranges of values. One range represents logic level **1** while the other range represents logic level **0**. Within each range, the exact signal level is of no significance. In logical gates all inputs and outputs are digital signals.

Analog voltages, on the other hand, are voltages whose precise value is always significant. Such analog voltages may be fixed in value or may make excursions through a continuous range of values. There frequently occurs a need for switches in circuits and systems involving analog signals, in which the opening and closing of the switches are to be controlled by digital waveforms. Circuits of this type are variously called *analog gates*, *transmission gates*, *linear gates*, *time-selection circuits*, etc., depending on the purpose to which the circuit is put. The switch-control digital waveform is referred to as the *gating signal*, the *control signal*, or the *logic input*.